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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,345	06/28/2001	Krishnamurthy Soumyanath	42390.P11206	8325

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EXAMINER	
NGUYEN, HAI L	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,345	SOUMYANATH ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,6,9,10,12,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,6,9,10,12,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on 12/27/02 has been received and entered in the case. The prior art rejections to the claims made in the previous Office Action are now withdrawn in view of Applicant's amendments and arguments. A new action on the merits appears below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 4, 6, 9, 10, 12, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sudo et al. (US 5,812,018; previously cited) in view of Chang (US 6,396,326).

With regard to claims 3 and 4, Sudo et al. discloses in Fig.1 a circuit, and a method of use thereof, comprising an input port (N10) having an input signal voltage (VBB); an output port (N15) having an output voltage (VPP); and a field-effect-transistor (M11) having a gate, a first terminal, and a second terminal; wherein the gate and the first terminal are each connected to the input port, and the second terminal is connected to the output port, the output voltage is inherently indicative of a local time-average maximum of the input signal voltage, and wherein in steady state the FET is coupled to operate in a sub-threshold region if the input signal voltage is stationary. Fig.1 of Sudo et al. meets all the claimed limitations except that Sudo et al. does not disclose the field-effect-transistor (M11) has a leakage current in excess of 1 micro ampere

per micron of device width as recited in the claims. Chang teaches in Fig.1 a circuit having field-effect-transistors, when their widths are large enough to prevent voltage build up at their drain causing electrical-over-stress. Therefore, the field-effect-transistors have leakage currents in excess of 1 microampere per micron of device width are seen to be obvious in view of Chang. In other words, the large of the width is the more leakage current. Therefore, it would have been obvious to one of ordinary skill in the art to implement the field-effect-transistors taught by Chang in order to prevent the voltage build up at their drain causing electrical-over-stress and damaging to the field-effect-transistors.

With regard to claims 9 and 10, and a method of use thereof, a circuit comprising an input port (N15) having an input signal voltage (VPP); an output port (N10) having an output voltage (VBB); and a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal; wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port. Furthermore, the limitation "the FET has a leakage current in excess of 1 micro ampere per micron of device width" is also met by the prior arts, note the above discussion with regard to claims 3 and 4.

With regard to claims 22 and 23, the claimed limitations in these claims are also met by the prior arts.

4. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Figs.1-4 in the present application, in view of Nakano (US 5,917,366; previously cited) and further in view of Chang.

With regard to claims 6 and 12, the prior art in Figs.1-4 shows a circuit, and a method of use thereof, to provide direct current (DC) offset correction to an input signal voltage, the circuit

comprising an input port (IN in instant Fig.4) having the input signal voltage; a field-effect-transistor (402) which can be replaced by a diode (202 in Fig.2); and a DC offset correction unit (406) responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage. Figs.1-4 of the prior art meets all the claimed limitations, except for a field-effect-transistor (702 in instant Fig.7) connected as recited in the claim. Nakano teaches in Figs.2-7 a circuit having field-effect-transistors (Q11-Q14) that are substituted for diodes. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that teaching of Nakano in the prior art (Figs.1-4) for the advantage of being able to reduce the threshold voltage of the field-effect-transistor. Also, it would have been obvious to one of ordinary skill in the art to connect the gate to either input or output which is in each case optimally matched to its application, i.e., direct the current to flow in a desired direction. Furthermore, the limitation "wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width" is also met by the prior arts, note the above discussion with regard to claims 3 and 4.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 703-306-9178 and Right Fax number is 703-746-3951. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HAI L. NGUYEN
PATENT EXAMINER
January 17, 2003